ABSTRACT OF THE DISCLOSURE

An arbitration circuit and a data processing system which ensure fair bus access are provided. An arbitration circuit (1) has a priority check block (21) and a round robin block (22). The priority check block (21) checks pieces of priority information provided from processors, specifies a processor that is presenting priority information with the highest priority, i.e. a processor with the highest priority level, and outputs the result of the check (CHK) to the round robin block (22). The round robin block (22), holding the results of the previous arbitration process, generates and outputs a processor selecting signal (SE) on the basis of the priority check result (CHK) and a round robin order generated from the previous results.